Heterogeneous 3D System-in-Package (SiP) Integration

Efficient and scalable integration using Intel's Embedded Multi-Die Interconnect Bridge (EMIB)

New class of FPGAs and MCPs to enable higher efficiency and flexibility

Enables convergence of process nodes and system functions into a single device

- Mix and match process nodes

Enables higher efficiency and flexibility

- Up to 1 Tbps full duplex on each EMIB Interface

Reduces size, weight and power
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EMIB - Intel’s Embedded Multi-Die Interconnect Bridge

Bump Images

Stratix 10 Packaging with EMIB Technology
AIB Overview

Supports peer-to-peer high bandwidth parallel communication

Versatile per-channel clocking in both directions

Streaming or transactional protocols can be implemented on top of AIB

AIB’s flexible IO cell permits arbitrary TX, RX, clock and control mapped by the protocol layer above

AIB Power Advantages

<table>
<thead>
<tr>
<th>Metric</th>
<th>SERDES</th>
<th>AIB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Energy (17pJ/bit)</td>
<td>12</td>
<td>11</td>
</tr>
<tr>
<td>Power (500Gbps example)</td>
<td>8.5W</td>
<td>0.5W</td>
</tr>
</tbody>
</table>

AIB Latency Comparisons

<table>
<thead>
<tr>
<th>Metric</th>
<th>JESD204C</th>
<th>AIB</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum line rate</td>
<td>32</td>
<td>2</td>
</tr>
<tr>
<td>Total Digital Delay TX</td>
<td>17.53</td>
<td>0.75 ns</td>
</tr>
<tr>
<td>Analog Delay TX</td>
<td>2</td>
<td>1 ns</td>
</tr>
<tr>
<td>PCB/Interposer Delay</td>
<td>0.31</td>
<td>0.06 ns</td>
</tr>
<tr>
<td>Analog Delay RX</td>
<td>2</td>
<td>1 ns</td>
</tr>
<tr>
<td>Total Digital Delay RX</td>
<td>20.62</td>
<td>0.75 ns</td>
</tr>
<tr>
<td>Total Delay</td>
<td>42.46</td>
<td>3.56 ns</td>
</tr>
</tbody>
</table>

The performance figures shown are optimized on Intel technology. Performance varies based upon system configuration.
Integrated Mixed Signal 2

Stratix 10 14nm Die (Monolithic)

Stratix 10 FPGA Tile

Backend Pipe 17G / 28G / 56G XCVR Tiles
Future System Concept: + Customer ASIC

- eASIC Inline Accelerator
- Extended Temp Memory
- Backend Pipe 28G / 56G / 112G XCVR Tiles
- Optical Interconnect
- Optical Interconnect
- Programmable FPGA Tile
- Custom ASIC Accelerator
- eASIC FPGA Replacement
- Future FPGA Replacement
- Memory Tile
- EMIB
Scalable Platform Strategy

Enable silicon programmability and hardened customization
- Optimized by market
- Further optimized by customer
- Tailored capability to desired combination of TTM, cost, power, integration

Reduce customer's R&D spend
- Consistent IP across pillars
- Software and package compatibility
- Maximizes reuse

Mix and match pillars and tiles
- Leverage chiplet strategy to integrate independent of node
- Blend pillar components for optimal power, performance, cost